A 10-Megasample-per-Second Analog-to-Digital Converter with Filter and Memory

In addition to analog-to-digital conversion, the HP E1430A addresses the problems of gain ranging, anti-aliasing protection, frequency band selection, triggering, data buffering, and multichannel synchronization.

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The Hewlett-Packard E1430A is a VXIbus-based analog-to-digital converter (ADC) module containing a high-dynamic-range, 23-bit-resolution, 10-MSa/s (megasamples-per-second) ADC, a family of octave-spaced anti-aliasing filters, a complex frequency shifter, and a 8-Mbyte FIFO buffer memory. It is designed to provide maximum performance and flexibility for capturing a bandlimited continuous analog signal in a format compatible with digital computers.

According to Nyquist's sampling theorem, any signal confined to a finite frequency bandwidth can be completely represented by a sequence of discrete samples taken at a rate of at least twice the signal bandwidth. If we are interested only in a finite time segment of the analog signal, all the necessary information is contained in a finite number of these samples taken from the appropriate segment of the sequence. In the absence of additive measurement noise we could theoretically represent the signal with infinite precision, although this would require infinite precision for each discrete sample. However, all analog measurements have some level of additive noise, which limits the amount of signal information available. Therefore, it is only necessary to store each sample with sufficient finite precision to retain the available signal information in the presence of the additive noise.

In other words, it is theoretically possible to completely determine a finite time segment of a bandlimited analog signal, to the extent allowed by additive measurement noise, by collecting a finite number of finite-precision samples of the signal. To maintain complete generality in capturing such a signal, the signal bandwidth, center frequency, start time, and time duration should all be independently specifiable. The HP E1430A offers a wide range of independent choices of all of these parameters while guaranteeing that the sample rate and data precision are sufficient to characterize the signal. The HP E1430A also minimizes the amount of additive measurement noise to preserve as much signal information as possible.

The HP E1430A is much more than an analog-to-digital converter. It also addresses the problems of gain ranging, anti-aliasing protection, frequency band selection, triggering, data buffering, and multichannel synchronization.

Module Description

The HP E1430A is implemented as a single-slot, C-size VXIbus module,\(^1,2\) as shown in Fig. 1. The primary analog connections are the three BNC connectors on the front panel, which are for the analog input signal, an external clock, and an external trigger. The four SMB connectors on the front panel provide the capability of sending synchronizing signals from one VXIbus mainframe to another mainframe containing additional HP E1430A modules.

![Fig. 1. HP E1430A analog-to-digital converter module.](image-url)
Fig. 3. Analog signal conditioning equivalent circuit.

Fig. 2. Block diagram of the HP E1430A ADC module.

The rear panel contains the standard VXIbus connectors, which are used for programming and reading data from the module. The HP E1430A complies with the VXIbus register-based protocol. Status lights are provided to indicate when the module is being accessed via the VXIbus backplane or when the input range is exceeded, producing an overload in the ADC.

Fig. 2 shows a functional block diagram of the HP E1430A module.

**Analog Signal Conditioning**

It is common practice at audio frequencies to provide high-impedance balanced differential inputs for ADC modules. However, maintaining good frequency response to a bandwidth of 4 MHz requires the use of a terminated transmission line to drive the input. The HP E1430A implements a 50-ohm pseudo-floating input as shown in Fig. 3. The cable ground is isolated from chassis ground by 50 ohms in parallel with a 0.04-µF capacitor. This is sufficient impedance to break up low-frequency ground loops, maintaining the key benefit of a differential input. At high frequencies where ground loops are no longer a problem, the 0.04-µF capacitor shorts out the common-mode signal, reducing the impact of common-mode feedthrough at high frequencies. The resistor damps out resonances of the input cable inductance with the cable-to-chassis capacitance.

Diodes are placed between the grounds to protect against damage and to satisfy safety concerns arising from high common-mode voltages. The result is an input termination that maintains good flatness to 4 MHz, suppresses low-frequency ground loop pickup, reduces high-frequency common-mode feedthrough, and eliminates unsafe high common-mode voltages.

Opening S1 under program control causes the input signal to be ac coupled through a 0.2-µF capacitor. This makes possible the measurement of low-level ac signals in the presence of a large dc offset. Programming S2 to the grounded position provides a 0-volt reference so that the offset DAC can be programmed to eliminate any dc offset in the input amplifier.

The gain or attenuation of the input amplifier is programmable in 6-dB steps so that sinusoidal input signals ranging from −32 dBm to +28 dBm can be scaled to produce a full-scale sine wave at the ADC. The noise added to the signal by the HP E1430A is −136 dB/Hz relative to full scale (dBfs/Hz) for the −14-dBm and higher ranges. It is −128 dBfs/Hz for the −20-dBm and lower ranges. This represents a 14-dB noise figure in the −32-dBm range. Most ADC modules have fixed, high-level input ranges requiring the user to provide low-noise external amplification.

**Anti-Aliasing Filter**

Since the normal ADC sample rate is 10 MHz, a complete representation of the input signal can be achieved only for bandwidths up to 5 MHz. To eliminate the possibility of higher-frequency components causing ambiguous results as a result of aliasing, all signal components above 5 MHz need to be removed before sampling occurs. The analog anti-aliasing filter in the HP E1430A is flat to 4 MHz and rejects signals above 6 MHz by at least 110 dB. Thus the 0-to-4-MHz frequency range of the sampled signal will be alias-free. The analog filter transition band from 4 MHz to
6 MHz affects the flatness and allows some aliasing in the sampled signal frequency range of 4 MHz to 5 MHz. In some applications a complete, unambiguous representation of a continuous signal may not be necessary, or the user may have additional information about the signal to allow a valid interpretation of the aliased components. In those cases anti-aliasing filtering may not be necessary, and the analog filter may be bypassed. This programmable mode allows the user to take advantage of the full 20-MHz sampler bandwidth. The anti-aliasing filter bypass mode should be used with caution and is not recommended for normal operation.

**Sampling ADC**

The heart of the HP E1430A is a precision ADC that generates 23-bit outputs at sample rates up to 10.24 MHz. The amplitude resolution is far in excess of the converter’s analog noise. Thus, the effects of finite quantization levels can be completely ignored, leaving the main error mechanisms, which are random white noise and linearity errors. For each sample the random error has a Gaussian amplitude distribution with an rms level of −70 dB relative to a full-scale sine wave. The random error for each sample is essentially uncorrelated with previous samples, meaning that the spectral energy of the noise is uniformly distributed across the 5-MHz Nyquist band. Therefore, the noise can be expressed as −137 dBfs/Hz. With the input amplifier noise included, the overall HP E1430A noise level is −136 dBfs/Hz (−128 dBfs/Hz for input ranges < −20 dBm). This low noise density is comparable to the best available ADCs at any sample rate.

In many applications, random errors can be filtered, averaged, or otherwise processed to reduce their impact on the final result. In these applications the deterministic signal-related errors—that is, distortion components—may limit the resulting accuracy unless they are significantly lower than the −70 dB broadband noise level. The HP E1430A achieves distortion errors of −80 dBfs to −110 dBfs depending on the level and dynamics of the applied signal. The graph shown in Fig. 4 shows the worst-case harmonic level for sinusoidal inputs of various levels. This distortion performance is considerably better than traditional ADCs in the 10-MSa/s class.

A more complete discussion of ADC errors and how the HP E1430A minimizes them is given in the October 1993 Hewlett-Packard Journal article titled “A 10-MHz Analog-to-Digital Converter with 110-dB Linearity,” publication number 5962-9494E.

**Zoom and Decimation Filtering**

For changing the signal bandwidth and center frequency, the HP E1430A provides a complex frequency shifter (zoom) and a complex low-pass filter. Both functions are implemented digitally with proprietary Hewlett-Packard high-speed ICs to achieve real-time operation. A Block diagram of the digital signal processing is shown in Fig. 5.

The local oscillator generates cosine and sine waves with spurious components smaller than -110 dBc and frequency resolution better than 10 µHz. These are then multiplied by the incoming signal to produce the real and imaginary components of the down-converted complex baseband signal. The complex baseband signal is then filtered to the desired bandwidth by separately filtering the real and imaginary components.

Bandwidth choices are provided with a cascaded chain of digital low-pass filters, each of which reduces the bandwidth by a factor of two. With the ADC Sample rate, $F_s$, set to the standard internal 10-MHz rate, the available bandwidth choices are ±5 MHz, ±2.5 MHz, ..., ±0.149 Hz around the programmed LO frequency. Each of the filters has ±0.35-dB amplitude flatness to 75% of its indicated corner frequency and has >105-dB rejection for signals above 125% of its indicated corner frequency. Because of the sharp cutoff, the time-domain step response of the filters has approximately 20% overshoot. Also, since the filters are not linear-phase, the time-domain impulse response is not symmetric. In time-domain applications...
where overshoot and/or impulse response symmetry are important the user can apply additional signal processing to achieve the desired filter response. Although the HP E1430A does not include this compensation filtering, all the necessary signal information is preserved to accomplish it within a host computer or signal processing module.

Once the signal bandwidth is reduced below $\pm f_s/4$ the effective trigger time can be offset from the actual trigger event by programming a trigger timing offset. The pretrigger offset is limited to the physical depth of the FIFO memory. The post-trigger offset is limited to $2^{20}$ samples.

**Clock and Trigger Generation**

Normally the ADC clock is produced by a 10-MHz crystal oscillator inside the clock generation block. However, for applications requiring a customer-supplied sample clock, the HP E1430A can accept an external TTL clock signal at a front-panel connector. The ADCs of multiple HP E1430A modules can be synchronized by programming them to use a common ECL clock line on the backplane. One of the modules can then be programmed as the clock master that drives this line. For systems involving more than one VXIbus mainframe, the backplane clock line can be extended to another mainframe by using the SMB connector on the front panel.

The trigger event used to start a measurement can be generated in four different ways: software trigger, external TTL, ADC threshold, and log magnitude. Any HP E1430A module can synchronously trigger multiple
HP E1430A modules via a shared sync line on the VXIbus backplane. This line can be extended between mainframes in the same manner as the ADC clock described above. All modules in a synchronous system are triggered on exactly the same ADC sample. All triggering modes support slope selection. The ADC and log magnitude modes also allow user selection of a trigger threshold, with hysteresis to prevent noise-generated false triggers on the wrong slope. The log magnitude triggering is based on the magnitude of the complex signal after zooming and filtering. The frequency selectivity of this mode is ideally suited to capturing low-level burst communication signals in the presence of larger interfering signals.

**Control**

All control of the HP E1430A module is accomplished by means of twenty-four writable and eighteen readable 16-bit registers mapped into the 16-bit VXIbus address space. The operating and service manual documents the function of each of these registers in detail. The module can be programmed from any VXIbus or VMEbus controller. The registers allow direct, high-speed access to all of the functions of the module.

To assist a programmer in using the HP E1430A effectively, the operating and service manual also includes documentation and a distribution disk or tape for a library of functions to facilitate programming the registers. These functions provide a C-language interface for setting up single modules and synchronous groups of modules spanning multiple VXIbus mainframes. Along with the low-level control functions, the library provides setup save and recall, autorange, auto-zero, and diagnostics. Also included are filter correction coefficients and a resampling algorithm to facilitate high-resolution, time-domain sampling. Because source code is included, the functions can be modified or translated to other languages. An executable program that invokes the diagnostic functions is included so that users with a supported controller can test the HP E1430A without writing any code.

For users who are accustomed to a high-level ASCII control interface, the distribution disk or tape includes software that will configure an HP E1405B command module to respond to ASCII commands from a supported external controller. The commands conform to the SCPI (Standard Commands for Programmable Instruments) protocol. The HP E1405B interprets each SCPI command and performs the appropriate register read/write operations on the HP E1430A. A driver is provided to support the HP ITG (Interactive Test Generator) and HP VEE-Test interactive environments. Either of these environments can use this driver and SCPI commands to provide a virtual front panel on the computer screen for control of the HP E1430A. The ITG and VEE software environments are sold separately.

**Summary**

The primary features that set the HP E1430A module apart from a typical ADC module are its high accuracy, high sample rate, selectable anti-aliasing filters, selectable center frequency, deep FIFO memory, analog signal conditioning, triggering, and fast data transfers. These are important considerations in modern communications receivers, radar and sonar processors, and transient capture equipment. Before digital signal processing algorithms can be applied effectively to signals, those signals must first be captured accurately in digital form. The HP E1430A provides all the necessary capabilities to perform this function with a high degree of flexibility.

**Acknowledgments**

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**References**